a3 Sub B3

2) an n-type fourth impurity region; and

c) a first fixed potential is applied to said second impurity region and a second fixed potential higher than said first fixed potential is applied to said fourth impurity region.

Claims 12-19. (withdrawn from consideration)

REMARKS

Favorable reconsideration of the above-identified patent application in light of the foregoing amendment and the following remarks is respectfully requested.

REQUEST TO CONSIDER IDS: As a preliminary matter, Applicant requests that the examiner return an initialed copy of the Form PTO-1449 that was filed with the Information Disclosure Statement (IDS) accompanying the present application on its August 17, 2001 filing date.

STATUS. Claims 1, 6-7 and 11 remain active in the application, being amended to be better organized and easier to read and not for reasons related to patentability; Claims 2 and 3 canceled without prejudice or disclaimer as being incorporated into independent Claim 1; dependent Claim 5 is also canceled without prejudice or disclaimer; Claims 4, 8-10, and 12-29 are withdrawn from consideration as being directed to a non-elected invention.

THE JULY 2, 2002 OFFICE ACTION. In the Office Action dated July 3, 2002, the restriction requirement was made final; FIG. 11 was objected to as not being labeled "Prior Art"; the following art rejections were asserted:

- Claims 1-3, 5, 7: admitted prior art (APA)
- Claims 1-3, 5, 7: *Proc IEEE* article (Tsang *et al.*)
- Claims 6 and 11: APA or Tsang *et al.*, in the alternative

Applicant proposes to amend FIG. 11 to include the "Prior Art" legend as required by the examiner. Accordingly, reconsideration and withdrawal of the objection to the drawings are respectfully requested.

Applicant respectfully traverses the rejections based on both references (APA and Tsang *et al.*), amending the claims to be better organized and easier to read, and not to avoid prior art.

PRELIMINARY DISCUSSION. Briefly, the invention of Claims 1, 6-7 and 11 are supported by Applicant's FIGS. 1-4:

> The foregoing description {of FIG. 1} describes the example using the pn junction of the unused CMOS transistor 201 to observe fluctuation in potential of the ***gate electrodes*** 1 and 10 of the CMOS transistor 200.
>
> Fluctuation in potential of the source/drain region of the CMOS transistor 200 can be observed as well. Figs. 2 to 4 are schematic views showing structures at a section of a modification of the semiconductor device according to the first preferred embodiment.
>
> - Fig. 2 shows the semiconductor device directed to observation of fluctuation in potential of the ***drain*** regions {3, 4} of the CMOS transistor 200.
> - Fig. 3 shows the semiconductor device directed to observation of fluctuation in potential of the ***source*** region {5} of the p channel MOS transistor 120.
> - Fig. 4 shows the semiconductor device directed to observation of fluctuation in potential of the ***source*** region {2} of the n channel MOS transistor 110.[1]

Thus, it is seen that the illustrative, non-limiting embodiments shown in FIGS. 1-4 provide the ability to measure, by fluctuations in potential, all of: the gate electrodes, and the drain and source regions, of a semiconductor device (that is, all of elements 2, 3, 4 and 5).

Claim 1 has been amended to include the limitations 2 and 3 (which, with Claim 5, are canceled without prejudice or disclaimer); Claim 1 has also been amended to include recitations relating to a first MOS transistor:

---

[1]Specification; paragraph bridging pages 13 and 14 (emphasis, reference numerals {}, and paragraph breaks have been added to make it easier for the examiner to apprehend the principle behind the disclosed exemplary embodiments); the claims are not limited to the particular features shown in the drawings or described in Detailed Description.

1. (Amended) A semiconductor device, comprising:

a) ***a second MOS transistor***, including a second gate electrode and ***a portion measured by fluctuation in potential***;

b) a wire having a first end and a second end, the second end being connected with said portion measured; and

c) ***an observation part*** including a ***pn junction*** irradiated with a laser beam to detect said fluctuation in potential, wherein:

1) said observation part includes ***a first MOS transistor*** having:

i) ***a source/drain region including a first impurity region*** of a first conductivity type, that is connected with said first end of said wire and that is formed within a second impurity region of a second conductivity type; and

ii) a first gate electrode that is ***electrically insulated*** from the second gate electrode; and

2) said ***pn junction*** includes said first impurity region.[2]

In preferred embodiments[3] providing support for the amendments to Claim 1, a gate electrode 10 of a "first" MOS transistor 120, and a gate electrode 21/30 of a "second" MOS transistor 111/121, are electrically insulated from each other.

Applicant submits that amended Claim 1 and its dependents distinguish the invention over the applied art.

ADMITTED PRIOR ART (APA). First, Applicant discusses how the admitted prior art (APA in Applicant's FIG. 11) does not disclose or suggest the combination of limitations that can be found in several claims.

The Office Action equates FIG. 11's peripheral circuit 50 with Claim 1's "portion to be measured by a fluctuation in potential."[4] This attempted correspondence is not proper, because

---

[2]Emphasis added.

[3]See especially page 9, lines 20-24 and FIGS. 1-4.

[4]Now amended to affirmatively recite that it is a —**portion [] measured** by a fluctuation in potential—.

peripheral circuit 50 is in no way tested by fluctuation in potential upon irradiation of a pn junction of an observation part. Indeed, the peripheral circuit merely drives portions of the transistors, as later explained with reference to FIG. 1:

> ...various potentials are outputted from the peripheral circuit 50 to the gate electrodes 1 and 10 to perform switching operation of the CMOS transistor 200.[5]

Moreover, the overall function of the circuit of FIG. 11 is very limited, allowing observation of fluctuation in potential only of the drain regions, and not of the source regions or gate electrodes:

> In the semiconductor device of the background art having the foregoing structure, while the LVP technique allows observation of fluctuation in potential of the drain regions acting as output terminals of the CMOS transistor 200 (the n^+ impurity region 3 and the p^+ impurity region 4), ***observation of fluctuation in potential of the gate electrodes 1, 10 and the source regions (the n^+ impurity region 3 and the p^+ impurity region 4) is <u>not</u> realized.*** As the n^+ impurity region 2 acting as a source region of the n channel MOS transistor 110 is the same in potential as the p well region 6, there occurs no reverse voltage to be applied between the n^+ impurity region 2 and the p well region 6. For the similar reason, there occurs no reverse voltage to be applied between the p^+ impurity region 5 and the $^-$ well region 7 of the p channel MOS transistor 120. Therefore, ***observation of fluctuation in potential of the source regions is <u>not</u> realized*** by the LVP technique. Further, as the gate electrodes 1 and 10 formed above the p-type semiconductor substrate 100 through the gate insulating film does not form a pn junction, ***observation of fluctuation in potential of the gate electrodes l and 10 is <u>not</u> realized*** either by the LVP technique.[6]

Accordingly, Claim 1 is not disclosed or suggested by the admitted prior art (APA).

Further, Claim 3 (now incorporated into Claim 1) requires that the observation part includes a first MOS transistor having the first impurity region as a source/drain region. In contrast, FIG. 11 shows that the region irradiated with laser energy is only a drain region, and not a source/drain region as claimed. Thus, the subject matter of former Claim 3 shows an advantage

---

[5]Specification; page 12, lines 1-2.

[6]Background of the Invention; paragraph bridging pages 3 and 4 (emphasis added).

of determining more potential faults more specifically, an advantage not provided by the admitted prior art, as noted in Applicant's specification:

> In the semiconductor device according to the first preferred embodiment, observation of fluctuation in potential of the ***gate*** electrodes 1 and 10 acting as input terminals of the CMOS transistor 200 is realized as well observation of fluctuation in potential of the ***drain*** regions (the n^+ impurity region 3 and the p^+ impurity region 4) acting as output terminals of the same. ***As a result, the failed part can be determined more specifically as compared with the semiconductor device in the background art.***[7]

Therefore, Claim 1 (Amended) should be allowable for the same reason that Claim 3 should have been allowed.

The semiconductor device of Claim 1 (Amended) includes a second MOS transistor having the portion that is measured by fluctuation in potential. The Office Action indicates (with reference to the rejection of Claim 5) that MOS transistor 120 in the admitted prior art (APA) is the portion to be measured. However, APA FIG. 11's MOS transistor 120 and peripheral circuit 50 are distinct elements: MOS transistor 120 does not have a peripheral circuit 50. Accordingly, the APA does not disclose or suggest Claim 1.

What the APA discloses is:

> ...Therefore, when the power source potential 9 is outputted from the CMOS transistor 200, a reverse voltage is applied between the n^+ impurity region 3 and the p^- well region 6. The pn junction formed between the n^+ impurity region 3 and the p^- well region 6 is irradiated with a near-infrared laser beam 20 and intensity of a reflected light of the laser beam 20 is detected. As a result, fluctuation in potential of the n+ impurity region 3 can be observed.[8]

---

[7]Specification; page 12, lines 19-24 (emphasis added).

[8]Page 4, lines 9-15.

Thus, the APA provides a technique premised on a gate electrode 1 of MOS transistor 110 having a CMOS transistor 200, and a gate electrode 10 of MOS transistor 120 are electrically connected with each other through a wire 11.

In contrast to the APA, Claim 1 requires that the gate electrodes of the first and second transistors be electrically insulated from each other. Accordingly, even when the second MOS transistor (including a portion to be measured) is performing a switching operation, the first MOS transistor (that is part of an observation part) does not perform a switching operation.

Thus, the structure of Claim 1 is not disclosed in or suggested by the APA, and the rejection is submitted to be improper and should be withdrawn.

Finally, Claims 6 and 7 are allowable over the admitted prior art in view of the paragraph bridging pages 3 and 4 of the Background: FIG. 11's circuit merely permits measurement of drain regions and not gate electrodes (Claim 6) or source/drain regions (Claim 7).

Thus, Claims 6-7 and 9 should be allowable by virtue of their own recitations, in addition to the features of the claims from which they directly or indirectly depend. Therefore, reconsideration and withdrawal of the rejection based on the admitted prior art (APA) are respectfully requested.

TSANG *ET AL.* Applicant also traverses the rejections based on the Tsang *et al.* article, for the following reasons.

Claim 1 (Amended) requires a second MOS transistor to have the portion that is measured. The Office Action mentions, concerning the rejection of Claim 5, that a p-channel MOS transistor (a MOS transistor connected through an output wire to an n-channel MOS transistor illuminated by a laser pulse) includes a portion to be measured (actually an output

wire). However, Tsang's FIG. 18 shows that the p-channel MOS transistor does not have an output wire, and accordingly, Claim 1 is neither disclosed or suggested by the Tsang *et al.* reference.

Moreover, Tsang's FIG. 18 semiconductor device is a CMOS transistor, in which a gate electrode of an n-channel MOS transistor illuminated by a laser pulse and a gate electrode of p-channel MOS transistor are electrically connected, with a same voltage being applied to them; this contradicts the language of Claim 1 (Amended) requiring the gates to be electrically insulated from each other.

The Office Action equates Claim 1's "portion [to be] measured" with the output wire of the CMOS device in Tsang's FIG. 18. There is little description of FIG. 18, other than to state that a laser pulse is focused on a drain diffusion. Significantly, there does not appear to be any concrete discussion to support the Office Action's interpretation or assertion that the output wire is indeed a portion measured by fluctuation in potential. Moreover, Tsang's focusing of a laser pulse on a drain diffusion is similar to the irradiation of drain regions in admitted prior art FIG. 11 as discussed above, and does not suggest the comprehensive ability of the invention to measure gates, drains and sources.

Rather than disclosing the particular details Applicant's claims to a semiconductor device, the Tsang *et al.* article focuses on more general principles of optical methods for measuring switching activity from the backside of a chip,[9] including a laser voltage probe (LVP) method[10]

---

[9]See Tsang *et al.* Abstract.

[10]Id., page 1441, left column, first full paragraph; and the extensive discussion beginning age page 1454, left column, which discussion includes the portion focused on in the July 3, 2002 Office Action.

However, Applicant is not claiming all-optical methods for measuring switching activity, or even LVP approaches in particular. Instead, Applicant is claiming the combination of limitations recited in Claim 1; in this regard, it is well established:

> ...for anticipation under 35 U.S.C. § 102, the reference ***must teach*** every aspect of the claimed invention either explicitly or impliedly. Any feature not directly taught ***must be*** inherently present.[11]

> A claim is anticipated only if ***each and every*** element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." [citation omitted] "The ***identical invention*** must be shown in ***as complete detail*** as is contained in the ... claim. [citation omitted].[12]

> To establish *prima facie* obviousness of a claimed invention, ***all the claim limitations*** must be taught or suggested in the prior art. [citation omitted] ***All words in a claim*** must be considered in judging the patentability of that claim against the prior art. [citation omitted][13]

Applicant submits that this burden has not been met, in the Tsang *et al.* rejection. Accordingly, Claim 1 is submitted to be allowable.

Analogous to the rejection of Claim 3 (now incorporated into Claim 1) based on the admitted prior art, Tsang *et al.* disclose only laser probing using the drain, and not the more comprehensive source/drain region as claimed.

Concerning Claims 6 and 7, as mentioned above concerning Claim 1, Tsang's focusing of a laser pulse on a drain diffusion is similar to the irradiation of drain regions in admitted prior art FIG. 11 as discussed above, and does not suggest the comprehensive ability of the invention

---

[11]MPEP § 706.02(a), subsection entitled DISTINCTION BETWEEN 35 U.S.C. 102 AND 103 (emphasis added).

[12] MPEP § 2131 (emphasis added).

[13]MPEP § 2143.03 (emphasis added).

to measure gates (Claim 6), drains and sources--or, more flexibly, the source/drain region of Claim 7.

More specifically concerning Claim 6: a portion to be measured is a gate electrode of a second MOS transistor. Therefore, the semiconductor device of Claim 6 constitutes a structure in which a gate electrode and an observation part are connected by a wire, a structure that is not disclosed or suggested by the cited art.

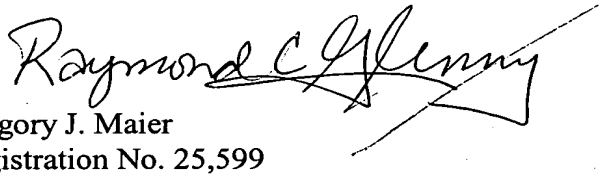
Like the APA, Tsang *et al.* are able to indirectly confirm whether a voltage exceeding (or not exceeding) a threshold is being applied to a gate electrode, by irradiating a pn junction with a laser beam. However, *the fluctuation in potential of the gate electrode* cannot be directly measured by either the APA or Tsang *et al.* Thus, in contrast to the APA or Tsang *et al.*, Claim 6 requires that the gate electrode and the observation part are connected through a wire, and it is possible to directly measure the fluctuation in potential of the gate electrode. Accordingly, Claim 6 has a structure that is neither disclosed in or suggested by the Tsang *et al.* reference, and, accordingly has an advantage that the Tsang *et al.* arrangement cannot provide. Accordingly, the rejections of Claim 6 is submitted to be improper, and reconsideration and withdrawal thereof are respectfully requested.

For at least the foregoing reasons, Applicant submits that all active claims are allowable. Moreover, because Claim 1 is allowable, all of Claims 2-19, including those that have been officially withdrawn from consideration, should be allowable as well. Therefore, reconsideration and withdrawal of the rejections, and allowance of Claims 1-19, are respectfully requested.

In view of the present amendment and in light of the foregoing discussion, it is respectfully submitted that the case is in condition for allowance. An early and favorable action to that effect is respectfully requested.

Respectfully submitted,

OBLON, SPIVAK, McCLELLAND,
MAIER & NEUSTADT, P.C.



Gregory J. Maier
Registration No. 25,599
Attorney of Record
Raymond C. Glenny
Registration No. 32,413

Phone (703) 413-3000
Fax (703) 413-2220

22850

I:\atty\RCG\212\212881us\212881-amd1.wpd

Marked-Up Copy
Serial No. 09/931,104
Amendment Filed on: 10/3/2002

ATTACHMENT

SHOWING CHANGES TO APPLICATION

1. (Amended) A semiconductor device, comprising:

a) a second MOS transistor, including a second gate electrode and a portion [to be] measured by fluctuation in potential;

b) a wire having [one] a first end and [the other] a second end, the second end being connected with said portion [to be] measured; and

c) an observation part [connected with said one end of said wire, wherein said observation part includes] including a pn junction irradiated with a laser beam to detect said fluctuation in potential, [and] wherein:

1) said observation part includes a first MOS transistor having:

i) a source/drain region including a first impurity region of a first conductivity type, that is connected with said first end of said wire and that is formed within a second impurity region of a second conductivity type; and

ii) a first gate electrode that is electrically insulated from the second gate electrode; and

2) said pn junction includes [a] said first impurity region [of a first conductivity type connected with said one end of said wire and a second impurity region of a second conductivity type].

2. (Canceled)

3. (Canceled)

4. (withdrawn from consideration)

5. (Canceled)

6. (Amended) The semiconductor device according to claim [5] 1, wherein:

said portion [to be] measured is a gate electrode of said second MOS transistor.

7. (Amended) The semiconductor device according to claim [5] 1, wherein:

said portion [to be] measured is a source/drain region of said second MOS transistor.

Claims 8-10. (withdrawn from consideration)

11. (Amended) The semiconductor device according to claim 1, wherein:

a) said first conductivity type is an n type and said second conductivity type is a p type;

b) said observation part further includes:

1) a second pn junction having a p-type third impurity region connected with said wire; and

2) an n-type fourth impurity region; and

c) a first fixed potential is applied to said second impurity region and a second fixed potential higher than said first fixed potential is applied to said fourth impurity region.

Claims 12-19. (withdrawn from consideration)